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jc713 U.S. PTO
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	42390.P4514D	Total Pages (all documents)	

First Named Inventor or Application Identifier
DOYLE

METHOD FOR DELAMINATING A THIN FILM USING NON-THERMAL TECHNIQUES

Express Mail Label No.	EM560643726US

jc542 U.S. PTO
09/416501
10/08/99

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] *Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. [X] Specification Total Pages [19]
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R&D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. [X] Drawing(s) (35 USC 113) Total Sheets [8]

4. [X] Oath of Declaration Total Pages [ ]
a. [ ] Newly executed (original copy)
b. [X] Copy from prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)

(Note Box 5 below)

i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in prior application, see 37 CFR 1.63(d)(2) and 1.33 (b).

5. [ ] Microfiche Computer Program (Appendix)

6. [ ] Nucleotide &/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 CFR3.73(b) Statement [ ] Power of Attorney (when there is an assignee)
9. [ ] English Translation Document (if applicable)
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
13. [ ] *Small Entity Statement(s) [ ] Statement filed in prior app Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. [ ]

* Note for Items 1 & 13: In order to be entitled to pay small entity fees, a small entity statement is required (37 CFR §1.27), except if one filed in a prior application is relied upon (37 CFR §1.28)

16. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information below & in a preliminary amendment:
[ ] Continuation [XX] Divisional [ ] Continuation-in-part (CIP) of prior application no: 09/107,398

Prior application information: Examiner: AHN D. MAI Group/Art Unit: 2814

For Continuation or Divisional Apps only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Signature		Date	10/7/99

Our Ref. No.: 42390.P4514 D
Express Mail No. EM560643726US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:)
)
Doyle)
)
)
For: METHOD FOR DELAMINATING)
A THIN FILM USING)
NON-THERMAL TECHNIQUES)
)

PRELIMINARY AMENDMENT

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Sir:

Please amend the above-identified divisional application as follows:

IN THE SPECIFICATION

After the title, please insert --This is a divisional of Serial Number 09/107,398, filed June 30, 1998.--

IN THE CLAIMS

Please cancel claims 1-13.

Please add the following claims:

--14. An apparatus comprising:

a first substrate with a semiconductor film formed thereon; and

a second substrate with a metal film formed thereon, said second substrate bonded with the metal film to said semiconductor film of said first substrate.--

--15. The apparatus of claim 14 wherein said semiconductor film demarcated from a rest of said first substrate by a damaged surface.--

--16. The apparatus of claim 15 wherein said damaged surface formed by ion implantation.--

--17. The apparatus of claim 14 wherein said metal includes a noble metal.--

--18. The apparatus of claim 14 wherein said first semiconductor film has a first oxide film formed thereon.--

--19. The apparatus of claim 14 wherein said metal film is formed on a second film of oxide formed on said second substrate.--

--20. An apparatus comprising:

a substrate;

a first oxide film formed on said substrate;

a metal film formed on said first oxide film;

a second oxide layer formed on said metal film; and

a semiconductor film formed on said second oxide film, said semiconductor film having a least one active device formed therein.--

21. The apparatus of claim 20 wherein said metal film includes a noble metal.--

REMARKS

Entry of the foregoing amendments prior to the initial examination of the above-captioned application is requested.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: October 7, 1999

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Our Ref.: 42390.P4514D
Express Mail No. EM560643726US

UTILITY APPLICATION FOR UNITED STATES PATENT

FOR

METHOD FOR DELAMINATING A THIN FILM USING NON-THERMAL TECHNIQUES

Inventor(s): DOYLE

Prepared by:

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BACKGROUND INFORMATION

(1) Field of the Invention

The present invention generally relates to fabrication of semiconductor devices. More specifically, the present invention relates to fabrication of integrated circuits that utilize pre-fabricated transistor layers.

(2) Description of Related Art

Modern integrated circuits are generally made up of a silicon substrate containing millions of active and passive devices including transistors, capacitors, resistors, etc. Until recently, the semiconductor industry's focus was on reducing the two dimensions, (X-Y)in a Cartesian system of coordinates, of the transistors to reduce the size of the integrated circuit. However, as integration in two dimension has become more and more difficult due to limitations of lithography tools, the exploitation of the third dimension (Z dimension in a Cartesian a system of coordinates) has become increasingly attractive.

Figure 1 illustrates a conventional integrated circuit 100 that includes a substrate 102 (typically made of silicon) onto which a very large number of active devices (transistors 104) are fabricated. Transistors 104 are intercoupled therebetween and to other devices, therefore forming various circuits, by way of an interconnect system that includes metal lines (106). The metal lines may further be connected to other circuits. The various circuits formed are further coupled, by well-known techniques, to

bond pads 108 of the integrated circuit. Transistors 104 are therefore located on a single layer of silicon at the bottom of the integrated circuit. When the dimension of the gates of transistors 104 goes some way beyond 193 nanometers, which is shortest wave length of the light used presently in the present day photolithography process, integration of transistors becomes problematic as lithography tools that are utilized in the process of fabrication of these transistors reach the limit of their performance. One solution to increasing integration without further having to minimize transistors' gates dimensions and thus without resorting to new lithography tools, is to build up further layers of transistors in a third dimension (Z dimension) as illustrated in Figure 2.

Figure 2 illustrates an integrated circuit that includes a first silicon substrate (base substrate 202) onto which are built a first layer (film) 205 of active devices 204. A second layer (film) 206 of active devices 208 may be envisioned as being further built in the Z dimension (vertically in the Figure). Interconnect lines 207 intercouple the active device 208 of second layer 206 to the active devices 204 of first layer 205. The second layer 206 of active devices 208 may be coupled to the outside world via bond pads 210.

In the display area (imaging) attempts have been made to integrate transistors in the third dimension. For example, some digital cameras use chips that have at the bottom thereof (at the base silicon substrate) transistors for logical operations and on top of those transistors are built display sensors. For example, CMOS

sensor arrays may be built in the third dimension and used as light sensors. However, these transistors do not have good conducting properties, and therefore their performance is weak.

The second layer transistors are not made of a single-crystal silicon but are made of a polycrystalline silicon or amorphous silicon. The problem in providing a second layer of active devices (transistors) made of single silicon crystal is that the fabrication of the second level of transistors requires processing steps that are performed well beyond the temperature that the interconnect system may withstand. For example, at 400° or 450° Celsius, the metal lines begin to melt. It is desirable to provide an integrated circuit that utilizes at least two layers of transistors that offer competitive performance at lower costs. It is desirable to provide an integrated circuit with a second level of transistors in the Z dimension made of a single crystal.

BRIEF SUMMARY OF THE INVENTION

The present invention provides a method for forming an integrated circuit. A semiconductor film is formed onto a first substrate. A metal film is formed onto a second substrate. The second substrate is bonded with the metal film onto the semiconductor film of the first substrate. A first layer of transistors is formed onto the semiconductor film. The second substrate is removed at a temperature within a low temperature range. The semiconductor film with the first layer of transistors is bonded to a second layer of transistors of a third substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, aspects, and advantages of the present invention will become more fully apparent from the following Detailed Description, appended claims, and accompanying drawings in which:

Figure 1 illustrates a cross-sectional view through a conventional integrated circuit;

Figure 2 illustrates a cross-sectional view through an integrated circuit with two layers of transistors, one above the other;

Figure 3 illustrates a cross-sectional view through a substrate onto which hydrogen is implanted;

Figure 4 illustrates a cross-sectional view through the first substrate with a film formed as a result of the ion implantation;

Figure 5 illustrates a cross-sectional view through the first substrate with a layer of oxide formed on top of the film;

Figure 6 illustrates a second substrate with a layer of metal formed on top of the second substrate;

Figure 7 illustrates a cross-sectional view of the first substrate with a film and a layer of oxide on which the second substrate with the metal film are bonded;

Figure 8 illustrates the assembly of Figure 7 turned upside down with the first substrate debonded;

Figure 9 illustrates the assembly of Figure 8 with active devices formed onto the film and subjected to a process of low-temperature annealing;

Figure 10 illustrates the assembly of Figure 9 with the film debonded from the second substrate;

Figure 11 illustrates a cross-sectional view through a third substrate with a layer of transistors onto which the film with its transistor is bonded; and

Figure 12 illustrates a flowchart diagram in connection with the embodiment of the process according to the present invention described herein.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth to provide a thorough understanding of the present invention. However, one having ordinary skill in the art should recognize that the invention may be practiced without these specific details. In some instances, well-known circuits, structures, and techniques have not been shown in detail to avoid obscuring the present invention.

Figure 3 illustrates a cross-sectional view through a first substrate 300, made of a semiconductor, onto which ions are implanted to form a thin film at a top portion 302 of the substrate. In one embodiment of the present invention described herein, the ions used for implantation are hydrogen ions. The energy of the hydrogen is chosen as a function of the thickness desired for the film. The higher the energy of the ions the thicker the film. The hydrogen ions may be 1E16-1E17 hydrogen.

Figure 4 illustrates a cross sectional view of substrate 300 with film 301 formed by way of the ion implantation process. Film 301 is demarcated by damaged surface 304 created by the implantation of hydrogen ions. The damaged surface 304 causes weakening of the bonds otherwise existing between what is now film 301 and the rest of first substrate 303. Later, when substrate 300 is heated at a certain temperature (typically 400° Celsius) film 301 detaches from substrate 300.

Figure 5 illustrates a layer of oxide 305 formed onto the film 301. Layer of oxide 305 is deposited onto film 301 so that

later in the process, when the first substrate with film 301 and oxide film 305 is bonded to a second substrate with a metal film 301 (not shown), the oxide 305 facilitates debonding of the film 301 from the second substrate with the metal film.

The oxide layer may be formed by deposition of a TEOS oxide, or a nitride layer. Alternatively, the oxide film may be thermally grown on surface 303 of the substrate 300 (Figure 3) before hydrogen implantation. The hydrogen introduced later on in the process during hydrogen implantation, reacts with the metal at the metal-oxide interface, and passivates the bonds that cause adherence of the metal film (not shown) to the oxide 305.

Figure 6 illustrates a cross-sectional view through a second substrate 310 onto which a metal film 312 is formed typically by sputtering. The metal film may be made of a noble metal such as platinum (tungsten) by way of example. The metal film could have any thickness from a few hundred Angstroms to a few thousand Angstroms or more. The metal film is bonded to a thin film of oxide (311) necessary to ensure that the metal does not form a silicide during later high temperature processing. This film can be deposited (TEOS) for example, or can be thermally grown on the silicon substrate 310. The metal film is utilized for its properties according to which if another structure is bonded to the metal film, and then later a hydrogen annealing step is performed to the bonded structures, it is easier to delaminate the other structures bonded to the metal film at the interface between the metal film and the other structure. The hydrogen bonds to the metal of this interface, terminating the adhesion bonds between

metal and oxide. Debonding may be performed smoothly by way of hydrogen annealing at a lower temperature that may not damage certain structures, such as active devices, later built on film 301.

Figure 7 illustrates a cross-sectional view of first substrate 300 with the first film 301 and oxide film 305 onto which the second substrate 310 with the metal film 312 are placed. The two substrates 300 and 310 with their respective films are then bonded by way of annealing (heating at a temperature of approximately 400° Celsius). One of the properties of noble metals such as platinum (tungsten) is that films, made of these metals are much easier debonded from silicon films such as 301 upon low-temperature hydrogen annealing, which is performed later in the process. When hydrogen is introduced in the environment, later on in the process (Figure 8), hydrogen diffuses through layer 301 and 312 causing the interface between these two layers to delaminate.

Next, in the process according to one embodiment of the present invention, the assembly illustrated in Figure 7 is heated at a temperature of approximately 400° Celsius that causes the film 301, with rough layer of oxide 305 to bond to metal film 312. The increased temperature of 400° Celsius also causes the rest of first substrate 303 to delaminate from the thin film 301. The reason is that the bonds between film 301 and the rest of first substrate 303 are weakened as a result of the hydrogen implantation discussed in connection with the cross-sectional view of the embodiment illustrated in Figure 3. The remaining

assembly, which includes thin film 301, oxide layer 305, oxide layer 311, metal layer 312, and the second substrate 310, is then flipped over such that film 301 is at the top of the assembly as shown in **Figure 8**. The film 301 of Figure 8 is then polished by a process of Chemical Mechanical Polishing (CMP), for example, and then active devices are formed in film 301 by conventional methods including etching, making trenches, ion implantation, forming the gate-oxide, etc.

Figure 9 illustrates the assembly of Figure 8 with first layer 314 of transistors 316 formed onto film 301. The remaining part 318 of film 301 has a thickness of approximately 2 micrometers while first layer 314 of transistors 316 also has a thickness of approximately 2 micrometers.

Figure 9 also illustrates the assembly subjected to a low temperature process of annealing. In one embodiment of the process of the present invention described herein, the low-temperature process of annealing is a process of hydrogen incorporation. The process described below describes hydrogen annealing as the method of hydrogen inclusion. However, other methods, such as hydrogen implantation, might also be used. Hydrogen annealing has the net effect of causing silicon film 301 to delaminate from the second substrate 310. The interface between silicon film 301 and the silicon substrate 310 with metal film 312 is replaced by bonds between hydrogen atoms that penetrate between metal layer 312 and oxide films 305. This new interface is easier to break down when the assembly is heated to a temperature of approximately 400° Celsius for 30 minutes during

hydrogen annealing. One advantage of the process according to the present invention is that hydrogen annealing is performed at a relatively low temperature at which transistors 316 of first layer 314 are not damaged.

Figure 10 illustrates two parts of the assembly resulting from the process of hydrogen annealing. The diffusion of hydrogen at the interface between film 301 (oxide film 305) and metal layer 312 reduces or eliminates the bonds between these two layers. Silicon film 301 (oxide film 305) and the metal layer 312, thus terminate on hydrogen instead of terminating on another layer, causing second substrate 310 to detach from its bonding with film 301 via metal 312.

The hydrogen annealing process is known in the art. A subject to be annealed is heated in a hydrogen ambient medium. The hydrogen atoms diffuse through film 301 and get to metal 312 causing the interface (between 301 and 312) to delaminate. The film of oxide 305 facilitates the debonding between the metal layer 312 and the film 301 as noble metals delaminate very well from oxide.

A third substrate 320 (carrier wafer) (shown in dotted lines) is then placed onto the transistor layer 314. The temperature of 400° Celsius causes bonding of the carrier wafer 320 to the transistors layer 314. The carrier wafer 320 that is used for supporting the transistor layer 314 may be the final substrate, or may be a temporary substrate (when this layer is later delaminated and bonded to another layer of transistors of a third substrate) (not shown).

After the second substrate 310 has been removed by way of the hydrogen annealing process, any remaining portion of metal or of oxide film 305 is stripped off the oxide film 305 by way of etching (dry etched in a fluorine based chemistry or can be polished off).

The embodiment of process according to the present invention then continues with placing film 301 bonded to carrier 320 on a layer 350 of transistors 352 of a third substrate 360 shown in **Figure 11**. Transistors 352 are interconnected by lines 354. The new assembly illustrated in Figure 11 is then heated at a temperature of 400° Celsius at which the film 301 bonds to the film 350 and the carrier 320 debonds from the film 301 of transistors 316.

Typically, the carrier wafer 320 is made of transparent materials such as quartz to allow alignment of the transistors of the two layers 314 and 350. The alignment between the two layers of transistors may be performed by well-known methods in the art. After alignment, the carrier 320 is debonded from the first transistor layer 314. At this stage the carrier 320 had served its purpose and can be stripped off.

The embodiment described above describes a system which incorporates two layers of transistors. It should be appreciated by persons skilled in the art that the process described herein may be used on a single layer of transistors to allow patterning of the underside of this single layer of transistor also. The underside patterning may be performed at the step corresponding to

Figure 9. In this case, the substrate 320 in Figure 10 becomes the final substrate, and transistors are fabricated on the now-exposed surface of 301, after the removal of the oxide layer 305.

Figure 12 illustrates a flowchart diagram in connection with one embodiment of a process for making an integrated circuit according to the present invention. The process starts at block 1202 from where it passes to block 1204. At block 1204 a semiconductor film is formed onto a first substrate. The process then passes to block 1206 where a metal film is formed onto a second substrate. The process continues to block 1208 where a second substrate is bonded with a metal film onto the semiconductor film of the first substrate. At block 1210 a first layer of transistors is formed onto the semiconductor film. The process continues to block 1212 where the second substrate is removed at a temperature within a low temperature range. The process then passes to block 1214 where the semiconductor film with the first layer of transistors is bonded to a second layer of transistors of a third substrate.

While the present invention has been particularly described with reference to the various figures, it should be understood that the figures are for illustration only and should not be taken as limiting the scope of the invention. Many changes and modifications may be made to the invention, by one having ordinary skill in the art, without departing from the spirit and scope of the invention.

CLAIMS

What is claimed is:

1. A method for making an integrated circuit the method comprising:

a. forming a semiconductor film onto a first substrate;

b. forming a metal film onto a second substrate;

c. bonding said second substrate with said metal film onto said semiconductor film of said first substrate;

d. forming a first layer of transistors onto said semiconductor film;

e. removing said second substrate at a temperature within a low temperature range; and

f. bonding said semiconductor film with said first layer of transistors to a second layer of transistors of a third substrate.

2. The method of claim 1 wherein said semiconductor film is formed by way of ion implantation.

3. The method of claim 1 wherein said metal film includes a noble metal.

4. The method of claim 1 further including, after removing said second substrate, bonding a carrier wafer onto said first layer of transistors.

5. The method of claim 4 wherein said bonding of said semiconductor film with said layer of transistors includes placing said carrier wafer with said first layer of transistors onto said transistor layer of said third substrate.

6. The method of claim 5 wherein said bonding of said semiconductor film further includes aligning said first layer of transistors with said second layer of transistors.

7. The method of claim 1 wherein said removing said second substrate at a temperature within a low temperature range is performed by way of hydrogen annealing.

8. The method of claim 2 further including, after bonding said second substrate, removing said first substrate.

9. The method of claim 8 wherein said first substrate is removed by heating an assembly that includes said first substrate with said semiconductor film and said second substrate with said metal film.

10. The method of claim 1 wherein, before said bonding of said semiconductor film with said first layer of transistors to a second layer of transistors, a carrier wafer is bonded to said semiconductor film.

11. The method of claim 1 wherein after forming a semiconductor film onto a first substrate a first oxide film is formed on said semiconductor film.

12. The method of claim 1 wherein said metal film is formed onto second oxide film deposited onto said second semiconductor.

13. The method of claim 1 wherein said first layer of transistors is replaced by a patterned layer.

ABSTRACT

A method for forming an integrated circuit is provided. A semiconductor film is formed onto a first substrate. A metal film is formed onto a second substrate. The second substrate is bonded with the metal film onto the thin film of the first substrate. A first layer of transistors is formed onto the film. The second substrate is removed at a temperature within a low temperature range. The semiconductor film is bonded with the first layer of transistors onto a second layer of transistors of a third substrate.

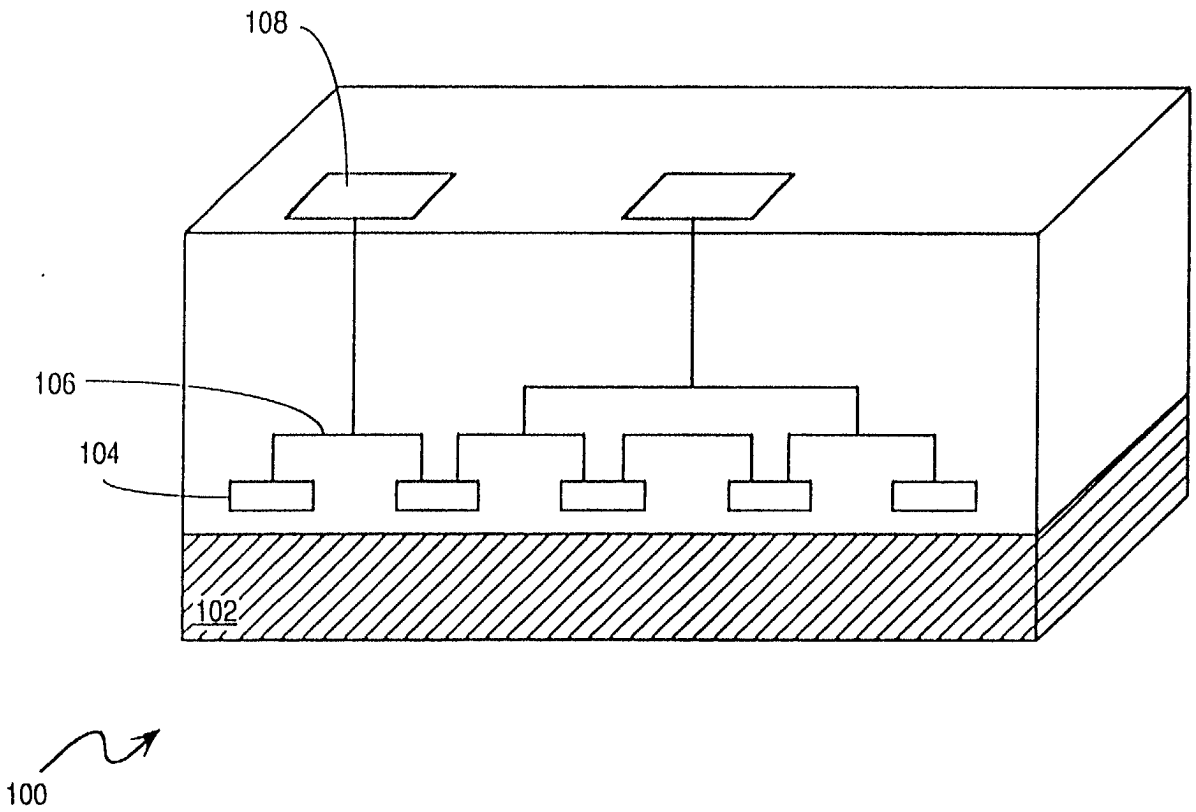

Fig. 1

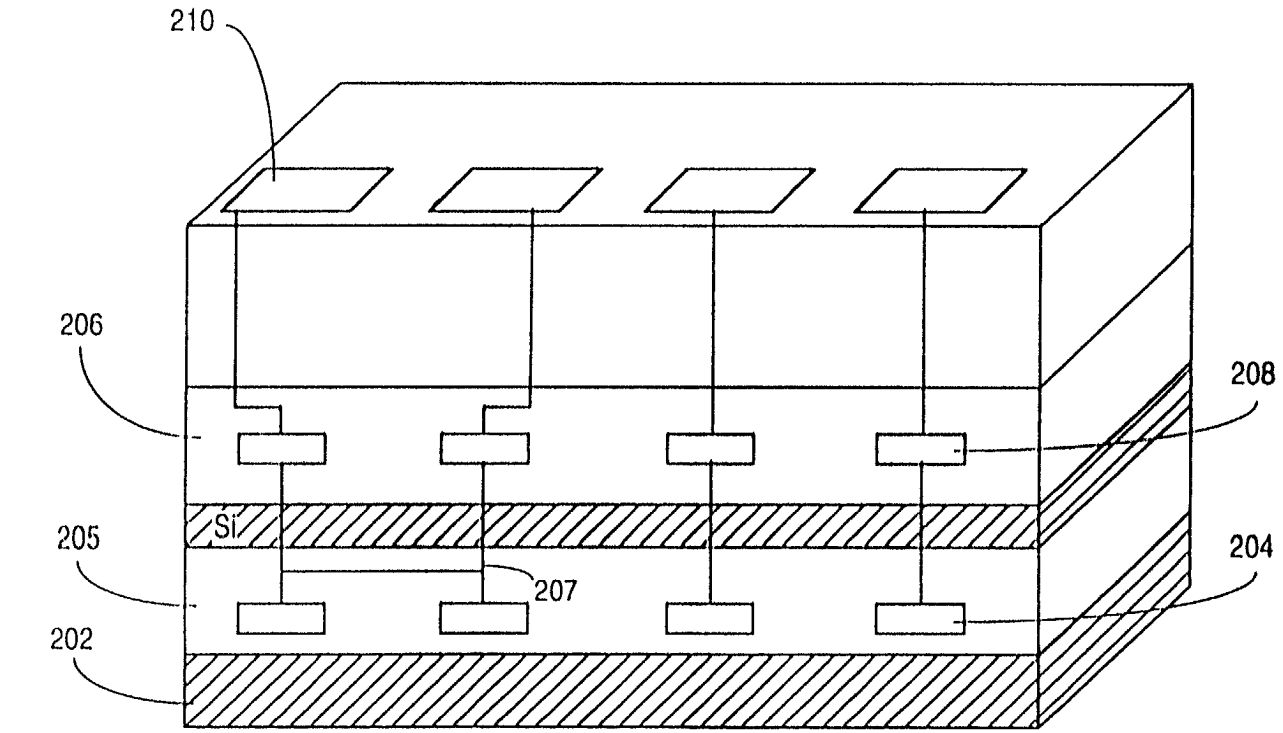

Fig. 2

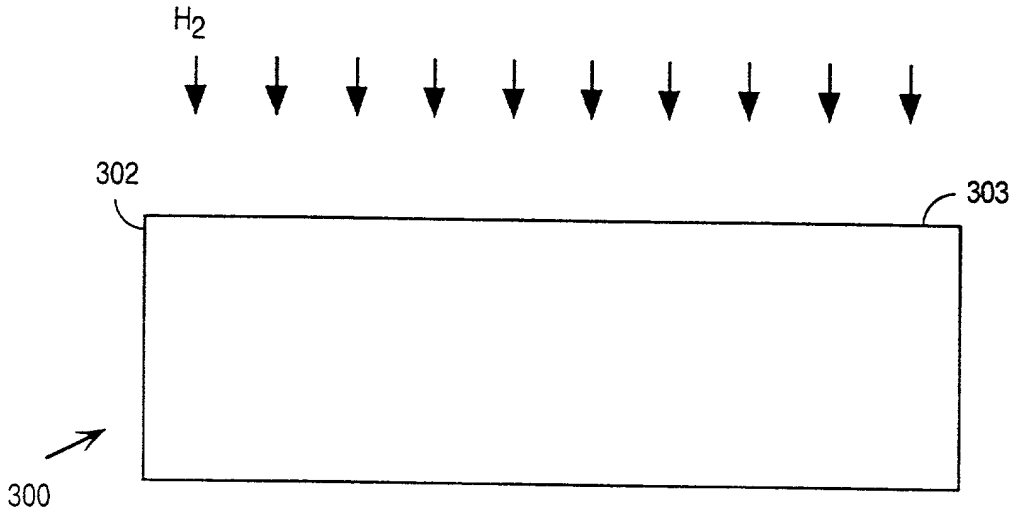

Fig. 3

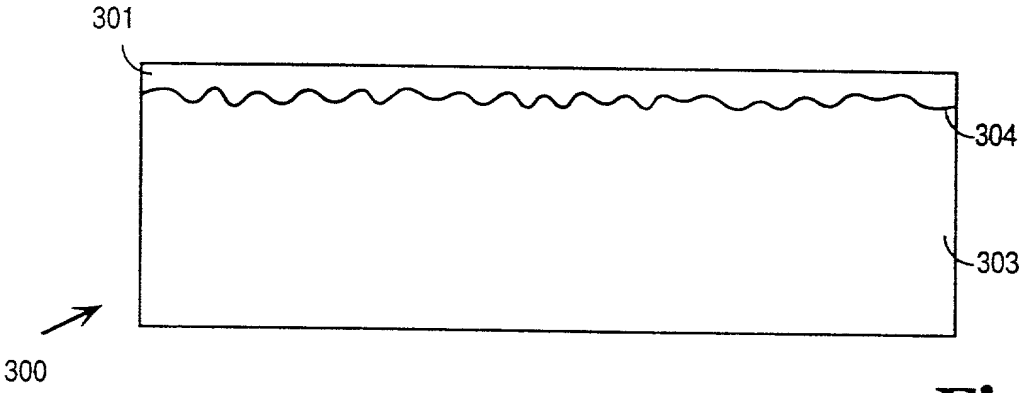

Fig. 4

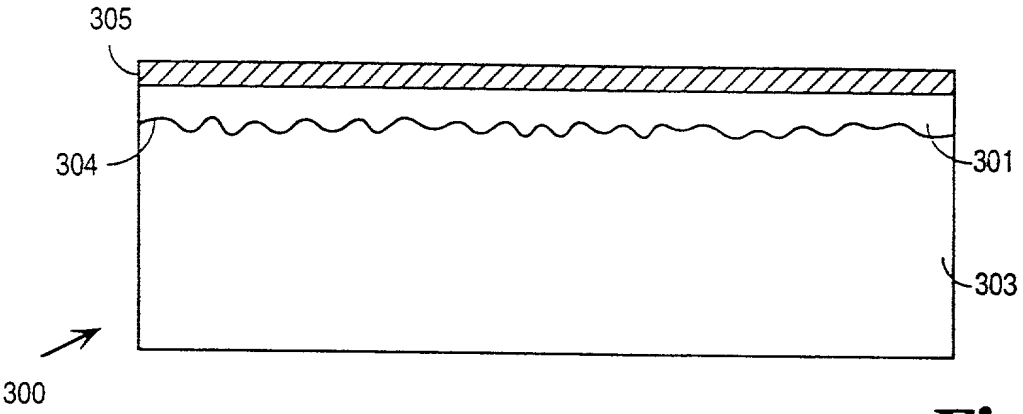

Fig. 5

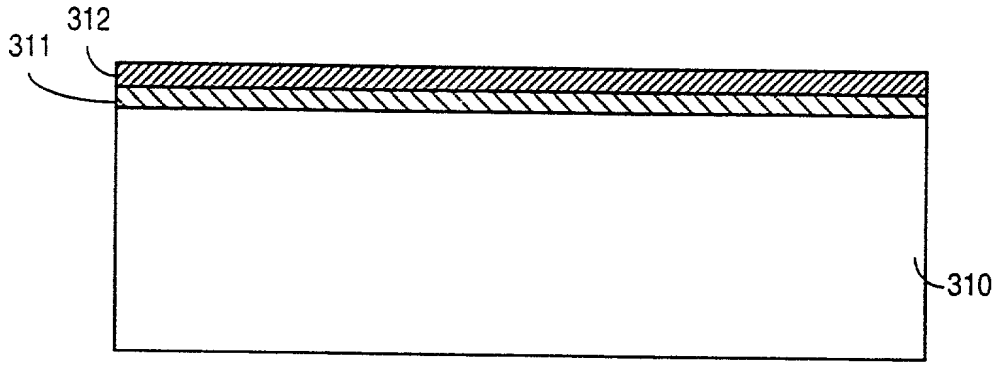

Fig. 6

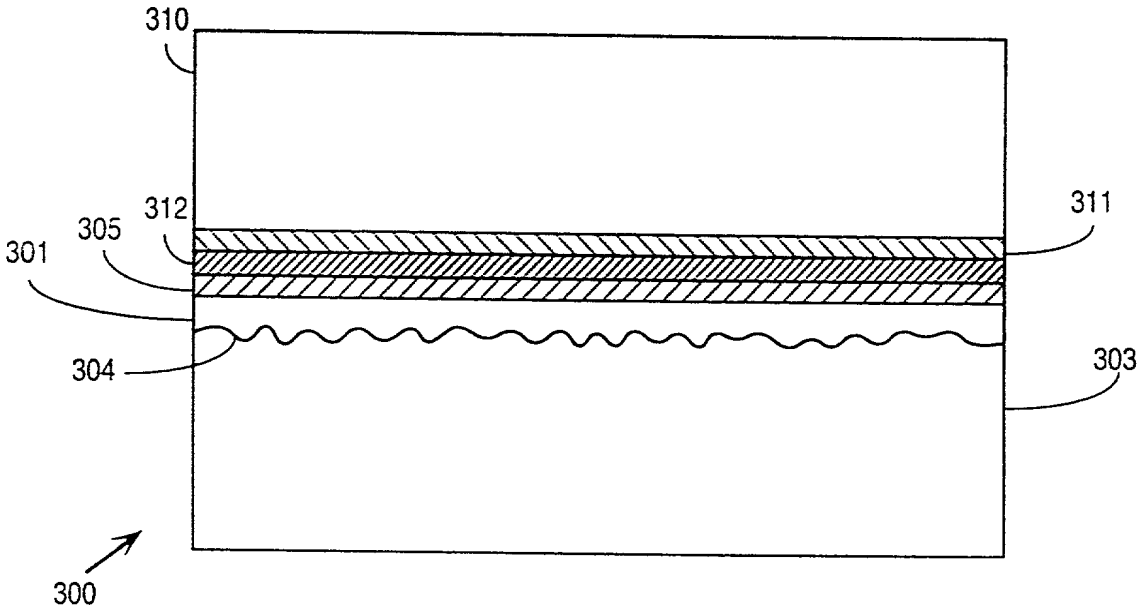

Fig. 7

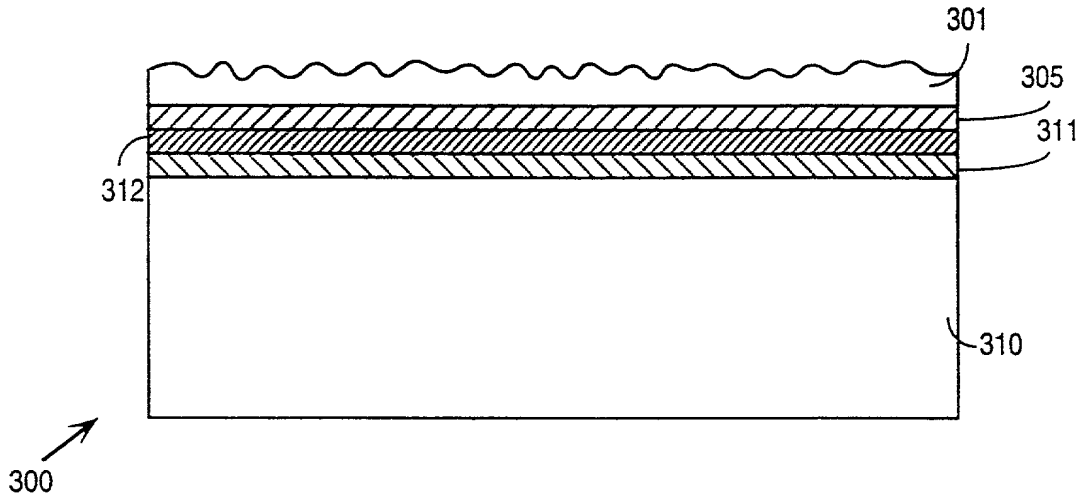

Fig. 8

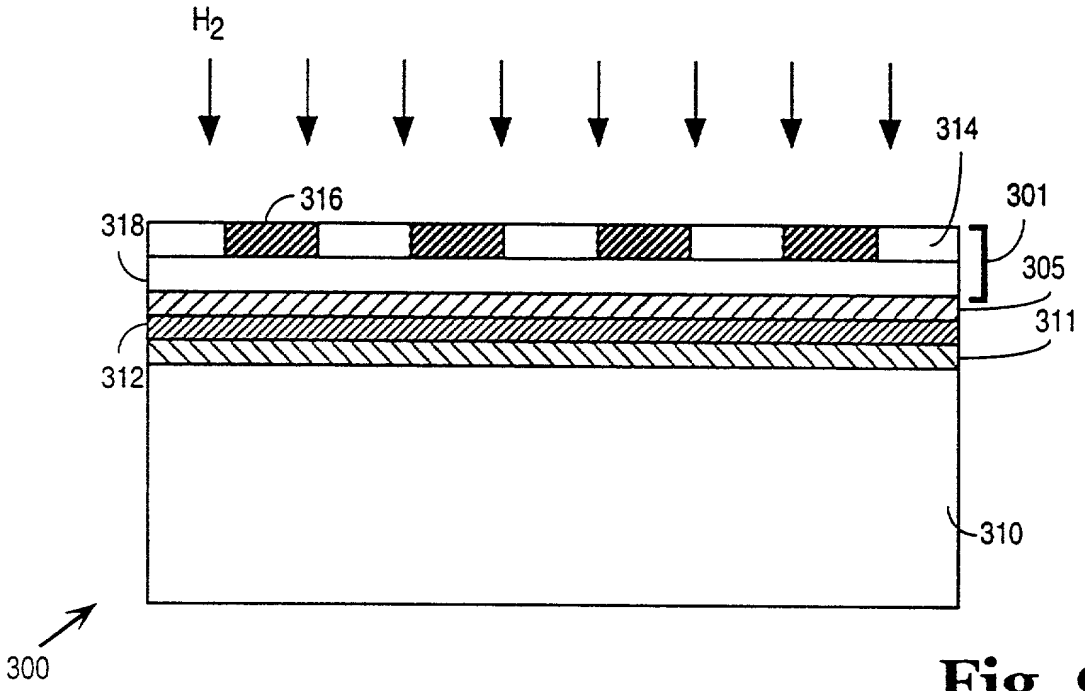
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Fig. 9

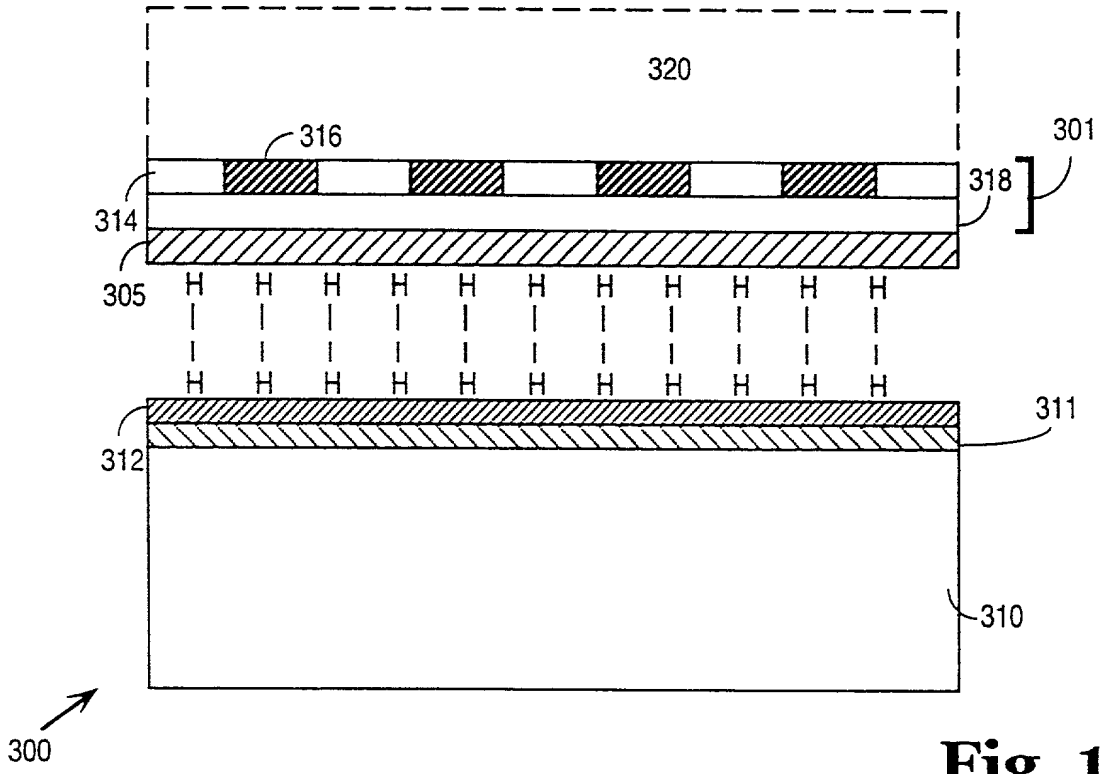
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Fig. 10

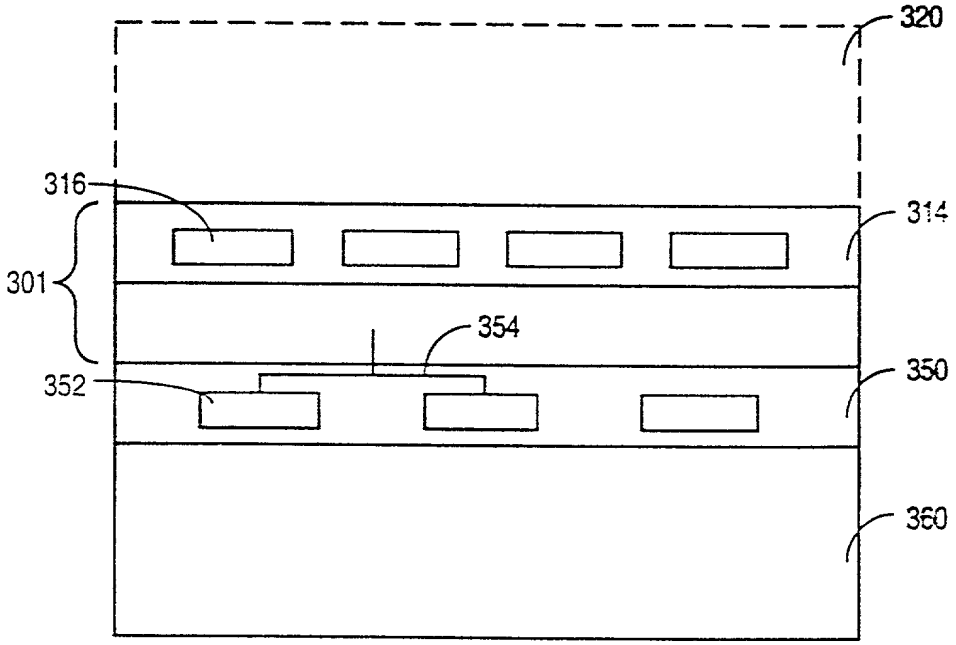

Fig. 11

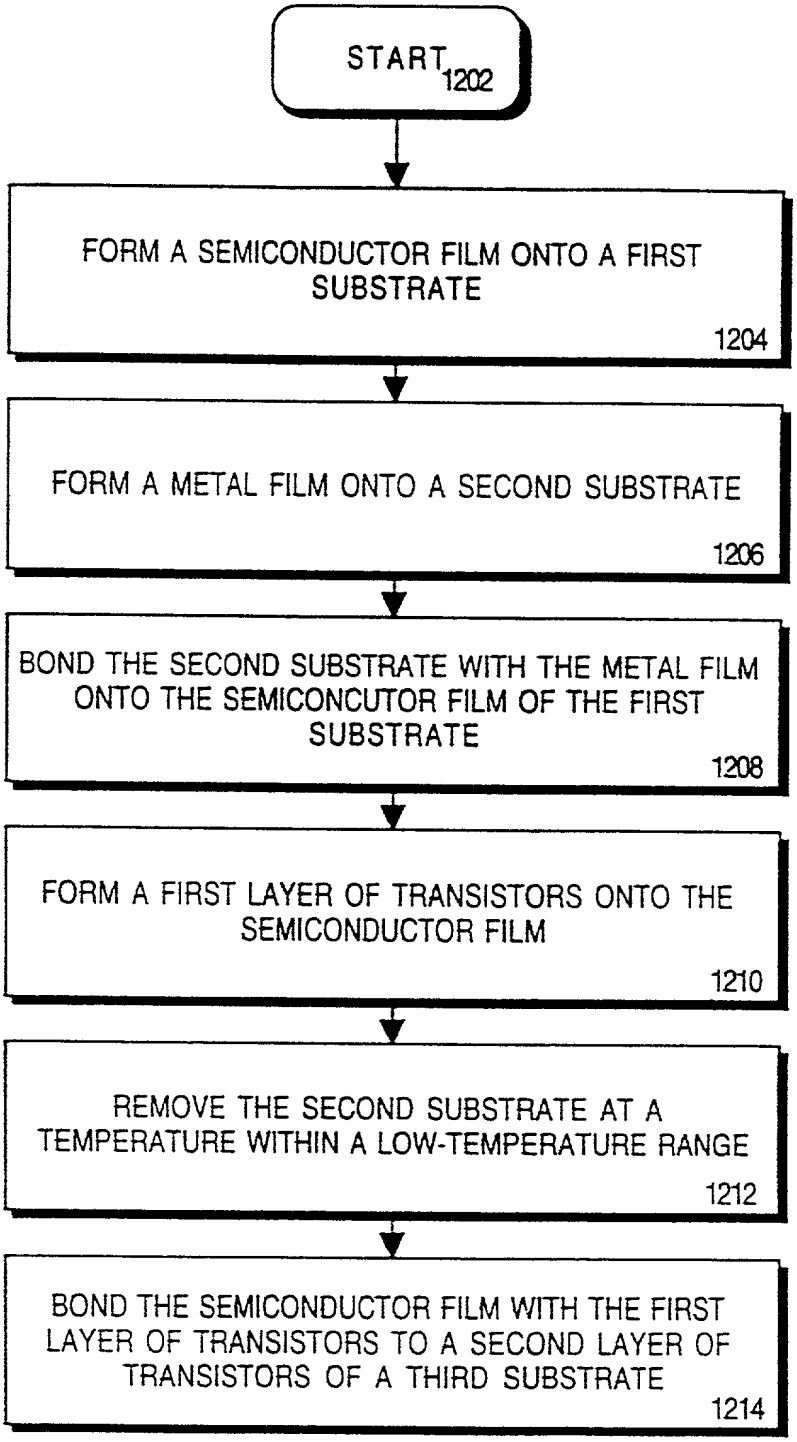
START
1202
FORM A SEMICONDUCTOR FILM ONTO A FIRST SUBSTRATE
1204
FORM A METAL FILM ONTO A SECOND SUBSTRATE
1206
BOND THE SECOND SUBSTRATE WITH THE METAL FILM ONTO THE SEMICONCUTOR FILM OF THE FIRST SUBSTRATE
1208
FORM A FIRST LAYER OF TRANSISTORS ONTO THE SEMICONDUCTOR FILM
1210
REMOVE THE SECOND SUBSTRATE AT A TEMPERATURE WITHIN A LOW-TEMPERATURE RANGE
1212
BOND THE SEMICONDUCTOR FILM WITH THE FIRST LAYER OF TRANSISTORS TO A SECOND LAYER OF TRANSISTORS OF A THIRD SUBSTRATE
1214

Fig. 12

Attorney's Docket No : 042390.P4514

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or any original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD OF DELAMINATING A THIN FILM USING NON-THERMAL TECHNIQUES - UTILITY

the specification of which
- ☐ is attached hereto.
- ☒ was filed on June 30, 1998 as United States Application Number 09/107,398 or PCT International Application Number _____ and was amended on September 3, 1998 (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, a firm including: Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, P41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. P42,442; William Donald Davis, Reg. No. 38,428; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Tarek N. Fahmi, Reg. No. P41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., P42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, P41,839; Willmore F. Holbrow III, Reg No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Tim L. Kitchen, Reg. No. P41,900; Michael J. Mallie, Reg. No. 36,591; Paul A. Mendonsa P42,879; Darren J. Milliken, P42,004; Thinh V. Nguyen, Reg. No. P42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch P43,021; Babak Redjaian, Reg. No. P42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; Geoffrey T. Staniford, P43,151; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. P42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, P43,237; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Amy M. Armstrong, Reg. No. P42,265; Robert Andrew Diehl, Reg. No. P40,992; and Edwin A. Sloane, Reg. No. 34,728; my patent agents, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor (given name, family name) Brian S. Doyle

Inventor's Signature _____ Date 9/6/98

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Our Ref. No.: 42390.P4514D
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:

Doyle

For: METHOD FOR DELAMINATING A THIN FILM USING NON-THERMAL TECHNIQUES

SUBMISSION OF FORMAL DRAWINGS

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

Submitted herewith are formal drawings, Figures 1-12.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 10/8/99

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